ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	Methodology for Verifying Multi-Cycle and Clock-Domain-Crossing Logic Using Random Flip-Flop Delays

Application Number :

Confirmation Number:

First Named Applicant: Hin-Kwai Lee

Attorney Docket Number: NM-103

Art Unit:

Examiner:

Search string: (5365463 or 5826061 or 6338127 or 5867691 or 4744084 or 6408265 or 6430731 or 5651012 or 5850355 or 5608645 or 5095454).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
SK	1	5365463	1994-11-15	Donath et al.	B1	703	019
SK	2	5826061	1998-10-20	Walp	B1	716	001
SK	3	6338127	2002-01-08	Manning	B1	711	167
SK	4	5867691	1999-02-02	Shiraishi	B1	713	400
SK	5	4744084	1988-05-10	Beck et al.	B1	714	033
SK	6	6408265	2002-06-18	Schultz et al.	B1	703	022
SK	7	6430731	2002-08-06	Lee et al.	B1	716	006
SK	8	5651012	1997-07-22	Jones	B1	714	724
SK	9	5850355	1998-12-15	Molnar	B1	703	015
SK	10	5608645	1997-03-04	Spyrou	B1	716	006
SK	11	5095454	1992-03-10	Huang	B1	703	019

Signature

Examiner Name	Date
Shamsher Poudel	7/25/06